

SHIELDED SEMICONDUCTOR PACKAGE WITH SINGLE-SIDED SUBSTRATE  
AND METHOD FOR MAKING THE SAME

Paul Hoffman

Doug Mathews

5

TECHNICAL FIELD OF THE INVENTION

The present invention relates to semiconductor chip packages, and in particular to a radiation-shielded semiconductor package with a single-sided substrate, and a method for making the same.

10

BACKGROUND OF THE INVENTION

Conventional and flip-chip integrated circuit packages using single- or double-sided epoxy laminate substrates are known. Such packages typically do not include electromagnetic interference shielding for the integrated circuit chip.

15

In some applications, it is desirable to shield the chip from electromagnetic interference. Electromagnetic interference is a particular problem in cellular telephones and other RF communication devices in which an antenna emits RF radiation which could affect the other circuitry operating in the phone. Electromagnetic interference shielding external to the package, which may consist of a metal casing surrounding the package, is costly and impractical. Incorporation of shielding into packages has remained problematic on a commercial scale.

20

SUMMARY OF THE INVENTION

Therefore, a need has arisen for a semiconductor chip package and packaging method that meets these challenges. In particular, a need has arisen for a shielded

25

semiconductor package with a single-sided substrate, and a method for making the same.

Accordingly, a semiconductor chip package is disclosed. In one embodiment, the package includes a substrate, a metallization layer formed on one side of the substrate and a semiconductor die mounted on the substrate. The semiconductor die is electrically connected to a portion of the metallization layer. A shield element is mounted on the substrate and electrically connected to a portion of the metallization layer. A package mold surrounds the semiconductor die and the shield element.

A method for assembling a semiconductor chip package is also disclosed. In one embodiment, the method includes providing a substrate having a metallization layer formed on a single side of the substrate, attaching a semiconductor die to the substrate, electrically connecting the semiconductor die to a portion of the metallization layer, mounting an electromagnetic interference shield on the substrate, and encapsulating at least a portion of the shield and the semiconductor die with a mold material.

An advantage of the present invention is that the package provides a shield against electromagnetic interference. Another advantage is that the package has the simplicity of manufacturing associated with single-sided substrates.

## BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present invention and for further features and advantages, reference is now made to the following description taken in conjunction with the accompanying drawings, in which:

5           FIGURE 1 is a vertical cross section of a first semiconductor chip package constructed in accordance with the present invention;

FIGURE 2 is a vertical cross section of a second semiconductor chip package;

FIGURE 3 is a side view of a shield element for use in the package;

FIGURE 4 is a top view of the shield element;

10           FIGURES 5 and 6 are close-up views of shield element legs;

FIGURE 7 is a side view of an alternatively-shaped shield element; and

FIGURE 8 is a top view of another alternatively-shaped shield element.

## DETAILED DESCRIPTION OF EXEMPLARY EMBODIMENTS

15           The exemplary embodiments of the present invention and their advantages are best understood by referring to FIGURES 1 through 8 of the drawings. Like numerals are used for like and corresponding parts of the various drawings.

FIGURE 1 is a vertical cross section of a semiconductor chip package 10 constructed in accordance with the present invention. Package 10 includes a package substrate 11, which may be a conventional epoxy laminate substrate. A die pad 14 and a set of bond fingers or pads 16 are formed on substrate 11 using conventional conductive layer fabrication techniques. Die pad and bond fingers 16 may be, for example, copper with or with gold and/or nickel plating. Substrate 11 is a single-sided substrate, meaning that a conductive layer including die pad 14, bond fingers 16 and  
20           conductive wiring (not shown) is formed on only one side of substrate 11. A  
25

semiconductor die 12 is mounted on a die pad 14 using a conventional die attach method and adhesive. Bond pads (not shown) on die 12 are electrically connected to respective bond fingers 16 by bond wires 18.

Package 10 includes a shield element 20 which shields semiconductor die 12 from electromagnetic interference. Shield element 20 may be made from any suitable metal, such as copper, nickel, chrome, stainless steel or other alloys, and may be plated with other metals to enhance corrosion resistance, improve solderability, or add to electrical shielding efficiency. For example, shield element 20 may be plated with gold, tin lead, indium, palladium, platinum and/or alloys of these or other metals. Shield element 20 is connected to selected bond fingers 16, and is grounded to provide an effective electromagnetic interference shield.

FIGURES 3 and 4 are side and top views, respectively, of shield element 20. Holes 22 are formed in the top and sides of shield element 20. Holes 22 allow mold compound to reach the interior of shield element 20 during formation of the package mold, as described below.

Holes 22 are appropriately sized relative to the wavelength of the radiation from which semiconductor die 12 is to be shielded. For example, holes 22 may have a diameter no greater than one-twelfth the predominant wavelength in the spectrum of electromagnetic interference.

No holes are formed in the central area of the top of shield element 20 (see FIGURE 4). This unperforated central area allows a vacuum pick-up head to pick and place shield element 20 during package assembly.

During package assembly, shield element 20 is placed on substrate 11 in electrical contact with selected bond fingers 16. As shown in FIGURE 3, shield element 20 includes legs 28 which contact the selected bond fingers 16. The open

spaces between legs 28 provide additional apertures for the entry of mold compound into the interior of shield element 20, thereby reduced the required number and/or diameter of holes 22 in shield element 20.

To assist in the alignment of a shield element 20 with bond fingers 16, each leg  
5 28 may have a concave lower surface as shown in FIGURE 5. The concave lower surface of leg 28 is shaped to receive the upper portion of a bond finger 16 (shown in cross section in the figure). Alternatively, as shown in FIGURE 6, leg 28 may have a convex lower surface designed to mate with a corresponding recess in the upper surface of a bond finger 16.

10 Shield element 20 may be attached to bond fingers 16 by means of solder or epoxy. Mold compound may then be injection-molded around shield element 20 to form package mold 24, which provides physical, electrical and thermal isolation for package 10. Package mold 24 may be formed from any one of a variety of commercially available mold compounds such as epoxidized ortho cresol novolac  
15 (EOCN), biphenyl (BP), dicyclopentadiene (DCPD) and multifunctional (MF) compounds available from a variety of manufacturers.

To reduce the possibility of air pockets remaining inside shield element 20 during injection molding, shield element 20 may have rounded corners as shown in the top view of FIGURE 4 and the side view of FIGURE 7. Alternatively, shield element  
20 20 may be circular in shape as shown in the top view of FIGURE 8. In this case the side view remains substantially the same as that shown in FIGURE 7.

Returning to FIGURE 1, bond fingers 16 may have solder pads 26 formed on their bottom surfaces. Alternatively, bond fingers 16 may be electrically connected to solder pads 26 by means of interconnect wiring (not shown) on substrate 11. In either

case, solder pads 26 are accessible from the bottom side of substrate 11 by means of through-holes or vias 27. Vias 27 may be formed by drilling through substrate 11.

Solder balls or bumps 29 are formed on solder pads 26 by conventional means. Solder bumps 29 may be, for example, conventional C4 solder bumps. Package 10 may be attached to a printed circuit board (not shown) by placing solder bumps 29 in contact with contact pads on the printed circuit board and reflowing solder bumps 29.

In an alternative embodiment, solder bumps 29 may be replaced by lands on the bottom surface of substrate 11. These lands may be electrically connected to bond fingers 16 by means of vias 27. However, in this embodiment, package 10 no longer has the simplicity of manufacturing associated with a single-sided substrate.

Referring to FIGURE 2, another embodiment of the present invention is shown. FIGURE 2 is a vertical cross section of a flip-chip semiconductor chip package 30 constructed in accordance with the present invention. Package 30, like package 10 previously described, provides integrated electromagnetic interference shielding for its semiconductor die.

Like package 10 described above, package 30 includes a package substrate 31, which may be a conventional epoxy laminate substrate. A die pad 34 and a set of bond fingers 36 are formed on substrate 31 using conventional conductive layer fabrication techniques. Substrate 31 is a single-sided substrate, meaning that a conductive layer including die pad 34, bond fingers 36 and conductive wiring (not shown) is formed on only one side of substrate 31. A semiconductor die 32 is mounted on a die pad 34 using a conventional die attach method and adhesive. Bond pads (not shown) on die 32 are electrically connected to respective bond fingers 36 by bond wires 38. Package 30 includes a shield element 40 which may have the same characteristics as shield element

20 previously described. For example, the leg shapes shown in FIGURES 5 and 6 may be used to achieve proper alignment of shield element 40 on substrate 31.

Package mold 42 may be created using conventional underfill techniques. Solder pads 44 are electrically connected to bond fingers 36 by means of interconnect  
5 wiring (not shown) on substrate 31. Solder bumps 46 may be formed on solder pads 44 by conventional means, allowing package 10 to be attached to a printed circuit board by reflowing solder bumps 46.

Although the present invention and its advantages have been described in detail,  
it should be understood that various changes, substitutions, and alterations can be made  
10 therein without departing from the spirit and scope of the invention as defined by the appended claims.